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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,168	11/13/2001	Ronald P. Novick	TRA-065	8054

36822 7590 11/14/2005

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EXAMINER	
WONG, WARNER	
ART UNIT	PAPER NUMBER
2668	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,168	NOVICK ET AL.	
	Examiner	Art Unit	
	Warner Wong	2668	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/13/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/13/01* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

The following claims are objected to because of the following informalities:

1. Claim 1, line 1: the acronym "UTOPIA" should be spelled out in its initial use as "Universal Test and Operation Physical Interface for ATM".

2. Claim 1, line 11: the limitation "**a** request signal" appears to refer to the same limitation recited on line 7. It should be reworded to "**the** request signal".

3. Claim 1, line 12: the limitation "**a** grant signal" appears to refer to the same limitation recited on line 8. It should be reworded to "**the** grant signal".

4. Claim 2, line 2: the numbering of step (e) is may be inconsistent since there are no other dependent claims with step (d). It should be labeled to step (d).

5. Claim 2, line 7: the limitation "**a** ready signal" appears to refer to the same limitation recited on line 3. It should be reworded to "**the** ready signal".

6. Claim 19, line 2: the acronym "PHY" should be spelled out in its initial use as "Physical Layer".

7. Claim 19, line 8: the acronym "CLAV" should be spelled out in its initial use as "Cell buffer Available".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 14 recites the limitation "a repeating frame bus" in lines 2-3, which has an ambiguous meaning and is not further described in the specification.

9. Claim 17 recites the limitation "a repeating frame bus" in lines 2-3, which has an ambiguous meaning and is not further described in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (4,596,012) in view of the Halsall ("Data Communications, Computer Networks and Open Systems", 1992) and Mizukoshi (6,307,858).

Regarding claim 1, Reed describes a method comprising:

a) coupling two bus masters to a single bus (col. 3, line 41-44, "The invention is embodied by .. a plurality of master stations 108 all of which are connected to a common information channel 110.");

b) designating one bus master the primary bus master and the other bus-master the secondary bus master (col. 4, lines 53-61, "Since each first time schedule is unique, there will be one master station 108 which will have a shortest first time schedule and thus reach its first time schedule before any other master station .. designating itself as the "active" [primary] master station..");

Reed lacks what Halsall (fig. 5.1) describes as a standard Data Link Control (DLC) layer connection-oriented handshaking:

c) DTE[1] (secondary bus master) sends L.CONNECT.request (request signal) to DTE[2] (primary bus master) and DTE[2] sends L.CONNECT.confirm (grant signal) to DTE[1], wherein

DTE[1] (is permitted to) transmit to the bus only after sending the L_CONNECT.request and receiving the L_CONNECT.confirm from DTE [2].

It would have been obvious to one with ordinary skill of art at the time of invention by applicant to use a handshaking procedure in communicating & granting bus controls between the primary and secondary bus masters. The motivation being that using a connection-oriented handshaking yields a reliable/guarantee communication between the bus masters (as opposed to best effort communication).

Reed and Halsall combined describe a multi bus master scheme for general/non-specific bus, which lacks what Mizukoshi describes as prior art for ATM bus network: an ATM layer device (bus master) connected to a UTOPIA bus (fig. 15 and col. 1, lines 23-29).

It would have been obvious to one with ordinary skill of art at the time of invention by applicant to apply the combined method of Reed and Halsall to that of an ATM network. The motivation being that the advantage of "multiple master controller succession system for bus access eliminates the network signal failure vulnerability of the central controlled bus" (Reed, col. 2, lines 42-45) may also benefit ATM UTOPIA bus networks.

11. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed in view of Halsall and Mizukoshi as applied to claim 1 above, and further in view of Moyer (5,416,910).

Regarding claim 2, Reed, Halsall and Mizukoshi describe all limitations set forth in claim 1. Halsall's DLC handshaking further describe:

e. DTE[1] (secondary bus master) sending a L.DISCONNECT.request (ready signal) to DTE[2] (primary bus master), (Halsall, fig. 5.1).

Reed, Halsall and Mizukoshi lack what Moyer describes:

[when alternate/secondary bus master is in operation (i.e. not malfunctioning)], the primary bus master (fig. 1, #12) is permitted to receive from the (UTOPIA) bus only when the secondary bus master (fig. 1, #16) sends a ready signal to the primary bus master (col. 5, lines 67-68 and col. 6 lines 1-2, "After receiving the qualified data bus grant the master-elect would assert the DBB* signal, thereby taking ownership of the data bus, and begin transferring data", where data transfer includes read/write).

It would have been obvious to one in the ordinary skill of art at the time of invention to specify the bus access scheme of Moyer in the combined method of Reed, Halsall and Mizukoshi. The motivation being that the primary bus master may avoid performing any processing of bus data which deems irrelevant to itself (i.e. when in use by others) and use such valuable processing for other means.

Regarding claim 3, Reed, Halsall, Mizukoshi and Moyer combined describes all limitations set forth in claim 2.

Reed further describes: [*in no circumstance*] the secondary bus master will fail to send a ready signal (i.e. malfunction) to the primary bus master (for more than one cell time) and requiring the primary bus master ignores the secondary bus master [since the secondary bus master will always reset] (col. 6, lines 36-39, "This logic occurs continuously as long as power is applied. If a circuitry malfunction occurs 303, then again the circuitry initialization [reset] means 302 is also exercised.", where secondary bus master will constantly reset until malfunction clears.)

Regarding claim 4, Reed, Halsall, Mizukoshi and Moyer combined describe all limitations set forth in claim 2.

Reed further describes that both the primary bus master and the secondary bus master may receive from the (UTOPIA) bus at the same time (fig, 2, #201 and col. 3, lines 15-18, where the flow diagram used by each slave and master station on the bus).

Regarding claim 5, Reed, Halsall, Mizukoshi and Moyer combined describes all limitations set forth in claim 4.

Reed further describes that each of the primary bus master and the secondary bus master screen out received cells which belong to the other (fig. 2, #202).

Regarding claim 6, Reed and Halsall and Mizukoshi combined describes all limitations set forth in claim 1.

Reed and Halsall lack what Moyer further describes: the secondary bus master transmits to the UTOPIA bus three clock cycles after the grant signal is received (D63-D0 "OUT" data appears 3 clock cycles after BG2* is asserted).

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to incorporate into the combined method of Reed, Halsall and Mizukoshi the Moyer's method with the above mentioned timing scheme. The motivation being that Moyer's method yields a fairness scheme to any instant (dual) bus master requesting the use of the bus (Moyer, col. 18-19, "Generally, multi-master systems depend on some sort of 'Fairness' arbitration to prevent any one bus master from monopolizing the external bus.")

Regarding claim 7, Reed, Halsall, Mizukoshi and Moyer combined describes all limitations set forth in claim 6.

Reed further describes: one of the three clock cycles is a dead cycle during which neither the primary bus master nor the secondary bus master controls the UTOPIA bus (col. 6, lines 46-55, "The negation [not using] by the current bus master of their independent bus request signal for a signal "dead" clock period, enables the arbiter 16 to 'fairly' select a new bus master-elect (i.e. alternate bus master 16) to assume ownership of the shared address bus 20, upon completion of the current bus transaction by the current bus master.")

Regarding claim 8, Reed, Halsall and Mizukoshi combined describes all limitations set forth in claim 1.

Reed, Halsall and Mizukoshi lack what Moyer further describes: the primary bus master sends a grant signal **according to an arbitration scheme** (col. 2, lines 50-53, "The bus grant signal notifies the first requesting bus master that the arbiter has selected the first request bus master to be a first bus-master elect.")

It would have been obvious to one with ordinary skill in the art at the time of invention by applicant to incorporate into the primary bus master of the combined method of Reed and Halsall the arbiter from Moyer's method. The motivation being that Moyer's method yields a fairness scheme to any instant (dual) bus master requesting the use of the bus (Moyer, col. 18-19, "Generally, multi-master systems depend on some sort of 'Fairness' arbitration to prevent any one bus master from monopolizing the external bus.")

Regarding claim 9, Reed, Halsall, Mizukoshi and Moyer combined describe all limitations set forth in claim 8.

Moyer further describes that the primary bus master and the secondary bus master alternate transmitting to the (UTOPIA) bus when both masters have cells to Transmit (col. 4, lines 66-68, "By asserting the BG2* signal, the arbiter 14 selects alternate bus master 16 to become the new master-elect.")

12. Claims 10-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of the Halsall and Mizukoshi.

Regarding claims 10 and 15, Moyer describes a bus access device (fig. 1, #12 or #16 as primary/secondary) comprising:

c) a control interface (fig. 1, #24, transfer control signals bus) for coupling to another bus access device (fig. 1, #16 or #12), said control interface.

Moyer lacks what Halsall describes as a standard Data Link Control (DLC) layer connection-oriented handshaking:

c) DTE[1] (secondary bus master) sends L.CONNECT.request (request signal) to DTE[2] (primary bus master) and DTE[2] sends L.CONNECT.confirm (grant signal) to DTE[1], wherein

It would have been obvious to one with ordinary skill of art at the time of invention by applicant to use the connection-oriented handshaking procedure at the control interface between the primary and secondary bus masters. The motivation being that using a connection-oriented handshaking yields a reliable/guarantee communication between the bus masters (as opposed to best effort communication).

Moyer and Halsall combined describe a multi bus master scheme for a general/non-specific bus network, which lacks what Mizukoshi describes as a prior art, a ATM network comprising:

a) a UTOPIA interface for coupling to a UTOPIA bus (inherent for any devices, including ATM layer interface [UTOPIA bus access device], connecting to the UTOPIA bus, fig. 15 and col. 1, lines 23-28);

b) an ATM layer interface for coupling to an ATM layer device (fig. 15, #1);

It would have been obvious to one with ordinary skills of art at the time of invention to specify the combined method of Moyer and Halsall into an ATM bus network with ATM components as per Mizukoshi. The motivation being that the advantage in the combined method where "the primary bus master can avoid performing any processing of bus data which deems irrelevant to itself (i.e. when in use by others) and use such valuable processing for other means" may also benefit an ATM bus network.

Regarding claim 11 and 16, Moyer, Halsall and Mizukoshi combined describe all limitations set forth in claim 10.

Halsall further describes the DLC handshaking (at the control interface):

DTE[1] (secondary bus master) sending a L.DISCONNECT.request (ready signal) to DTE[2] (primary bus master), (Halsall, fig. 5.1).

Regarding claim 12, Moyer, Halsall and Mizukoshi combined describe all limitations set forth in claim 10.

Moyer further describes that the primary bus master sends a grant signal **according to an arbitration scheme** (col. 2, lines 50-53, "The bus grant signal notifies the first requesting bus master that the arbiter has selected the first request bus master to be a first bus-master elect.")

Regarding claim 13, Moyer, Halsall and Mizukoshi combined describe all limitations set forth in claim 12.

Moyer further describes that, from the arbitration scheme, the primary bus master and the secondary bus master alternate transmitting to the (UTOPIA) bus when both masters have cells to transmit (col. 4, lines 66-68, "By asserting the BG2* signal , the arbiter 14 selects alternate bus master 16 to become the new master-elect.")

13. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Mizukoshi.

Moyer describes a method comprising:

a) coupling two bus masters (fig. 1, #12 & 16) to a single (data) bus (fig. 1, #22);

b) designating one bus master the primary bus master (fig. 1, #12) and the other bus-master the secondary bus master (fig. 1, #16);

c) the coupling in (a) is such that the primary bus master controls and polls (i.e. read at rising clock edge) the data (UTOPIA) bus until control is given to the secondary bus master (fig. 2, clock cycle 3 where D63-D0 asserting data "IN" , and col. 5, lines 67-68 and col. 6 lines 1-2, "After receiving the qualified data bus grant the master-elect would assert the DBB* signal, thereby taking ownership of the data bus, and begin transferring data", where data transfer includes read/write).

whereupon the secondary bus master controls and polls (read) the bus from where the primary bus master left off (i.e., continues to transfer [read/write] at a subsequent times where the previous bus master left off) (e.g., in fig. 2, clock cycle 6 the alternate bus master asserting data "OUT" on D63-D0, where in this example the transfer is a 'write').

Moyer describe a multi bus master scheme for a general/non-specific bus network, which lacks what Mizukoshi describes as a prior art, am ATM network with a UTOPIA bus.

It would have been obvious to one with ordinary skills of art at the time of invention to specify the method of Moyer with to the general (prior art) ATM network of Mizukoshi. The motivation being that the advantage in the combined method where "the primary bus master can avoid performing any processing of bus data which deems irrelevant to itself (i.e. when in use by others) and use such valuable processing for other means" may also benefit an ATM bus network.

14. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Mizukoshi and Microchip's 8-bit Parallel Slave Port (hereinafter referred to as the "Microchip IC".

Moyer describes a method comprising:

a) coupling two bus masters (fig. 1, #12 & 16) to a single (data) bus; (fig. 1, #22);

Moyer lack what Mizukoshi describes:

b) one bus master (ATM layer interface) polling the PHYS coupled to the bus (fig. 15, #1 as bus master, #2-0 to 2-M as PHYs, and col. 49-50, polling the PHYs);

It would have been obvious to one with ordinary skills of art at the time of invention to incorporate Moyer's multi bus master method in a general/non-specific bus into the ATM bus network of Mizukoshi. The motivation being that the advantage in the Moyer's method where "the primary bus master can avoid performing any processing of bus data which deems irrelevant to itself (i.e. when in use by others) and use such valuable processing for other means" may also benefit the ATM bus network.

Moyer and Mizukoshi lack what the Microchip IC describes:

c) maintaining a scoreboard (fig. 1, IBF input buffer full status bit) of each PHY indicating which PHYs asserted the CLAV line [in response to the most recent poll] (p.1, "The read-only status flag bit IBF is set if a received word is waiting to be read [for a particular PHY]");

d) neither bus master selecting a PHY unless the scoreboard indicates that the CLAV line was asserted (p.1, "When the external device performs either a read or a

write operation to the PIC16CXXX, interrupt flag will be set and the processor [bus masters] interrupted if bit PSPIE is set and interrupts are enabled", where the IBF bit is also set when the external device performs a 'write' [i.e. PIC16C16CXXX obtained a received word], and the bus master will not process (select the PHY) unless interrupted).

e) resetting the scoreboard entry for a PHY when either bus master selects the PHY (p.1 "Bit IBF is clear upon read of the input buffer latch.")

It would have been obvious to one with ordinary skills of art at the time of invention to incorporate Microchip IC's into the combined method of Moyer and Mizukoshi, each flagging data availability (a scoreboard) of a corresponding PHY. Such incorporation is well-known in the art. The motivation being that this (separate scoreboard) mechanism independently keeps track of the requests of multiple incoming I/O, as opposed to loading such functionality and processing to the processing device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 5:30AM - 2:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Warner Wong
Examiner
Art Unit 2668

WW

CHIEH M. FAN
PRIMARY EXAMINER